IJEW 国际工程期刊 International Journal of Engineering Works انجینئرنگ کاموں کا بین الاقوامی جرنل

International Journal of Engineering Works
ISSN-p: 2521-2419
ISSN-e: 2409-2770
Vol. 6, Issue 03, PP. 84-89, March 2019
https://www.ijew.io/

Modeling of Cascaded H-Bridge Multi-level Inverter Having Low Total Harmonic Distortion by using Equal Phase Distribution Method

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Received: 12 February, Revised: 01 March, Accepted: 05 March

***Abstract*—** Multi-level inverters' popularity over traditional inverters can be attributed to its low total harmonic distortion. Multi-level inverter is used both for high and low power applications. This study uses Equal phase method to analyze the total Harmonic distortion of 3, 5, 7 and 9 levels by using Cascaded H-Bridge configuration for such analysis. The total harmonic distortions of three, five, seven and nine levels are analyzed, studied and finally their output is compared through fast Fourier transform. Results are acquired by simulating Cascaded H-Bridge Multi-level inverter with MATLAB/Simulink. Simulation results reveal that total Harmonics Distortion reduces as voltage level is increased. Total harmonic distortion for 3, 5, 7 and 9 levels is 41.42, 39.46, 39.40 and 22.50 percent respectively.

***Keywords*—** Cascaded H-Bridge, Equal Phase method, MATLAB/Simulink, Switching Angle, Total Harmonic distortion (THD).

I. INTRODUCTION

Power electronics interface is needed to synchronize the power of renewable energy sources with that of grid in order to meet the requirement of grid integration. Different kind of grid tied inverters solves the issue of synchronization each associated with certain level of THD. Multi-level inverter (MLI) proves a good candidate with the ability to harness high quality waveform with low THD. The output waveform of multilevel inverter is much better because of multiple voltage levels if compare to two levels inverter which has such distortion comparatively higher. Also, there is no need of output filter for removing these distortions. With low switching frequency and absence of large output filter it is advantageous in minimizing cost, complexity and power losses. MLI uses many different topologies: Diode clamped MLI, flying capacitor MLI, H-Bridge MLI [1]. Total harmonic distortion can be reduced by varying pulse widths and phase delays of any level of inverter [1]. Total harmonic distortion of single phase 3-level and 5-level is analyzed by varying loads such as R-loads and RL loads. Both type of power i.e. active and reactive power is calculated and compared [2].

Multi-level inverter is better in terms of electromagnetic compatibility, low switching losses and high voltage capability. In recent years MLI got much higher consideration [3]. Multi-level inverter synthesizes voltage from different dc sources and separates them in case of cascaded H-bridge.

Three different topologies presented here: diode clamped, flying capacitor and cascaded H-Bridge; their functions, features, applications, configurations, operating principles and performances are discussed [3]. Multilevel inverter besides reducing harmonics and EMI also decreases the dv/dt stress on switches without the use of high frequency switching and thus lowering switching loses [4].

When these three configurations are compared, harmonic content in cascaded H-Bridge multilevel inverter is much lower as compared to diode clamped and flying capacitor, also the output waveform in cascaded H-Bridge is much better and more sinusoidal than the other two topologies under discussions. Harmonic contents decreases by increasing the output levels [5].

Different methods can be used to calculate the switching angles of multilevel inverter. Output voltage depends on firing of switching angles. For m level 2(m-1) switching angles are needed [5].

Devising of line voltage THD of MLI is proposed by analytical algebraic method with uneven dc generators. The conventional technique works in more of an approximate fashion, ignoring high order harmonics and formulating the THD with limited number of low order harmonics. Nine equations of a line voltage for five level inverters are presented to formulate a line THD and consider harmonics up to 10^6th order. The proposed model is based on speed, accuracy and simplicity and found accurate [6].

A model of three phase 5 level hybrid inverter with three cascaded H-Bridges and different DC sources is proposed [1]. The control signal is given through digital technique by FPGA controller. The prototype has been tested with different types of load such as 18W fluorescent lamp, induction motor of 1 HP and RL load. The results are obtained in terms of total harmonic distortion. Results show that THD voltage is between 15.6% and 18.3% for output line-line and phase

voltages having 5 levels, the output waveform of phase current is close to sinusoidal such that its THD current is between 2.7% and 4.2%. Nine levels inverter are simulated by using cascaded H-Bridge configuration and grid simulator. Sampling method of pulse width modulation is validated in this paper [7]. Two carrier frequencies are chosen 600 Hz and 2 kHz for experimental work.

A 13-level inverter is simulated with equal distribution of switching angle arrangement. As the name suggest it has 13 levels of output and consist of three cascaded H-Bridges per phase [10]. The proposed method has advantage of equal load distribution on each transistor thus preventing overheating.

By using different level of MLI, reduction in THD is studied in this paper. In second section of paper methodology has been discussed for different configurations in different levels of inverter. Equal phase method is used for measuring switching angles. In third section of paper simulation results are presented. Three, five, seven and nine levels inverter is simulated and results are gathered for discussions. In fourth section paper is concluded by comparing the THD of 3, 5, 7 and 9 level of inverter based on total harmonic distortion.

II. METHADOLOGY

Application of Multi-level inverter lies high voltage direct current. HVDC can be converter through MLI. Two level inverter has limitations for high power and high voltage applications. We cannot rely further on conventional two-level inverter. We have to switch to multi-level inverter for these applications. Two different electrically operated schemes can be connected by using MLI. The most appropriate topology is cascaded H-Bridge which allows to add up the voltages. The switches current and voltage stresses can be minimized by using this topology.

Total harmonic distortion has inversely relation with the voltage levels. Increasing voltage levels results in large number of components which hence increases the price and complexity but we have to compromise between smooth waveform and price [8]. Table 1 shows the number of switches and components used in different topologies of multi-level inverter [9].

Three level inverter has one H-Bridge and four main switches with a freewheeling diode. Five level inverter has two H-Bridges. Seven level inverter has three H-Bridges. Nine level inverter has four H-Bridges. We can synthesize three output levels in three level inverters as V, 0. –V. Five level inverter can synthesize five output voltage levels as shown in fig 1. Seven level inverter has seven output voltage levels i.e. -3V, -2V, -V, 0, V, 2V, 3V. Output of nine level inverter is shown in fig 2.

Fast Fourier transform is used for analyzing the total harmonic distortion. Cascaded H-Bridge has been used as it has less number of switches and also it does not require any clamping devices like capacitor and diodes [1].

Firing angles are formulated through Equal phase method. Switches are given a specific firing angles with a known pulse width. We need 2(m-1) switching angles for m level. There is increase of of power by (m-1) time of 2-level inverter in multi-level inverter [2].

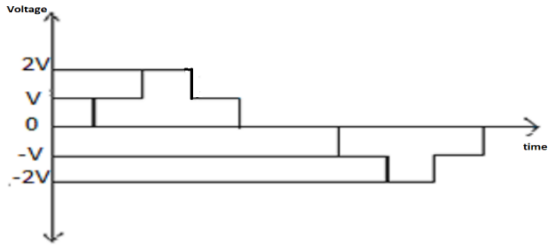

Figure 1. Output waveform of five level inverter

TABLE I. COMPARISON OF COMPONENTS OF 7 LEVEL INVERTER

Type of multilevel inverter	Number of switches	Clamping diodes	Flying Capacitors
Flying capacitor	12	-	15
Diode clamped	12	30	-
Cascaded H-Bridge	12	-	-

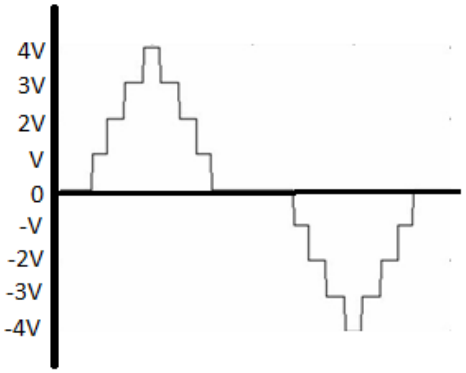

Figure 2. Output waveform of Nine level inverter

Main switching angles in the first quarter ( ) are

$$a_1,\ a_2, a_3, \cdots\cdots \quad (1)$$

In second quarter switching angles ( ) are

$$a_{(m+1/2)} = \pi - a_{\left(m-\frac{1}{2}\right)}, \pi - a_{\left(m-\frac{2}{2}\right)}, \cdots\cdots, \pi \quad (2)$$

Switching angles in the third quarter ( ) are

$$a_m = \pi + a_1, \pi + a_2, \cdots\cdots\cdots, \pi + a \quad (3)$$

Switching angles in the fourth quarter ( ) are

$$a_{(3m-1/2)} = 2\pi - a_{\left(m-\frac{1}{2}\right)}, \cdots\cdots\cdots, 2\pi - a_1 \quad (4)$$

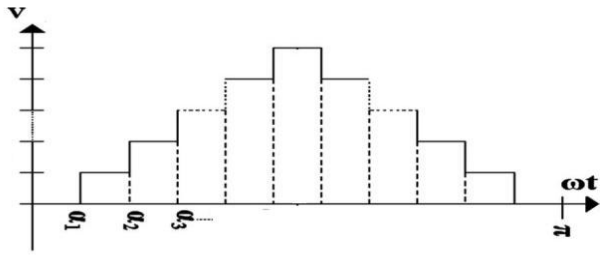

Figure 3. Multilevel output waveform

A. *Equal Phase Method:*

Equal phase distribution has been used for obtaining the switching angles. By using equal distribution method, the problem of unbalance loading in cascaded H-Bridge configuration is solved which increases the life time and prevent the switches from overheating. The main switching angle is obtained from:

$$a_i = i \times 180/m \quad (5)$$

Where m is the level of output voltage and i = 1, 2, 3…, m-1/2

III. SIMULATION RESULTS

3, 5, 7 & 9 level inverter is simulated using MATLAB/Simulink. The firing angles for switches correspond to a particular triggering pulse are provided using equal phase method from timing table. Total harmonic distortion is analyzed based on these simulation results.

A. *Three Level Inverter*

Equal phase method is used for Switching. In Fig 4 three level inverter has been shown by using four mosfets as switches to form an H-Bridge configuration. Output waveform can be seen in Figure 5. Total harmonic distortion has been analyzed here by using fast Fourier transform analysis and results are compared. In Fig 6 percentage of THD is shown, clearly limiting it to 41.42%, for equal phase method. In the positive half cycle S1 & S2 are closed keeping S3 & S4 open at the same time and thus providing a positive voltage at output. In the negative half cycle S1 & S2 are open to provide negative voltage at output whereas S3 & S4 are closed. Triggering pulses are provided from table 2 where control of multilevel inverter is given showing how to create a PWM signal for switches to operate and synthesize desirable output.

TABLE II. TIMING DIAGRAM OF THREE LEVEL INVERTER

Phase	**0**	**V**	**0**	**-V**	**0**
Switching Angle	60	120	240	300	360
Phase Delay	0.0033	0.0066	0.0133	0.0166	0.02
S1 & S2		30%			
S3 & S4				30%	

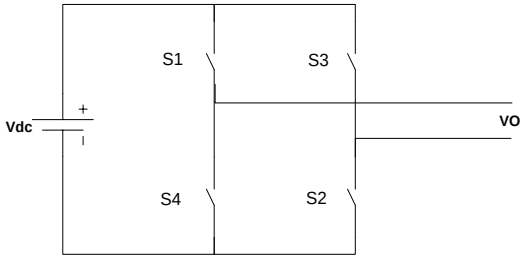

Figure 4. Simulink model of three level H-Bridge inverter

Fourier expansion of output voltage of squared natured waveform has three components: fundamental component, desired component and harmonic component. Magnitude of fundamental component depends directly on input dc voltage.

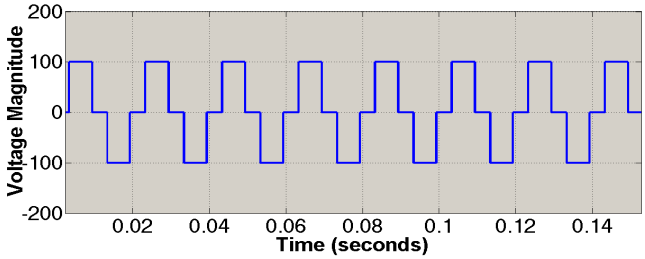

Figure 5. Output waveform of three level inverter

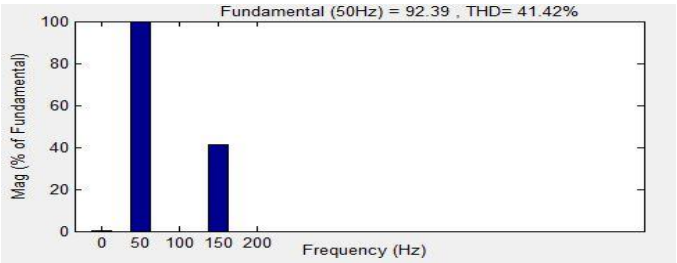

Figure 6. Total harmonic distortion percentage of three level inverter

B. *Five Level Inverter*

For five levels inverter, there are two bridges connected in series to make two H-Bridges interconnection having two separate DC sources. Equal phase method has been used for switching angles calculation. Eight mosfets are used to form two H-Bridge configuration as can be seen in Fig 8. THD as Fig 9 indicates is 39.46%.

For positive cycles S1, S2 & S6 are closed giving +V voltage. In order to get 2V, switch S5 will be closed with other switches. For negative switches S3, S7 & S8 are closed which gives –V, whereas for getting -2V switch S4 will be operated with other switches. Table 3 shows the timing table with firing angles and phase delays given.

Magnitude of fundamental component is inexorable, leaving no control to user, though constant, throughout the cycles. Magnitude of harmonic component depends in inverse fashion on order of harmonics. For square waveform results in odd harmonics.

TABLE III. TIMING TABLE OF FIVE LEVEL INVERTER

Phase	0	V	2V	V	0	-V	-2V	-V	0
Switching angles	36	72	108	144	216	252	288	324	380
Phase delay	0.002	0.004	0.006	0.008	0.012	0.014	0.016	0.018	0.02
S1, S2 & S6		30%							
S5			10%						
S3, S7 & S8						30%			
S4							10%		

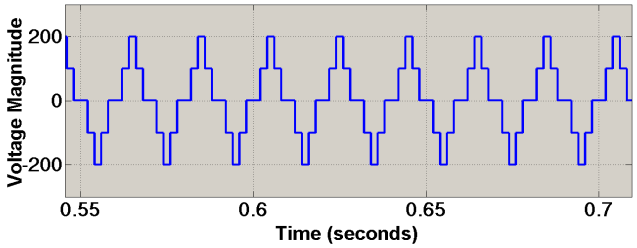

Figure 7. Output waveform of five level inverter

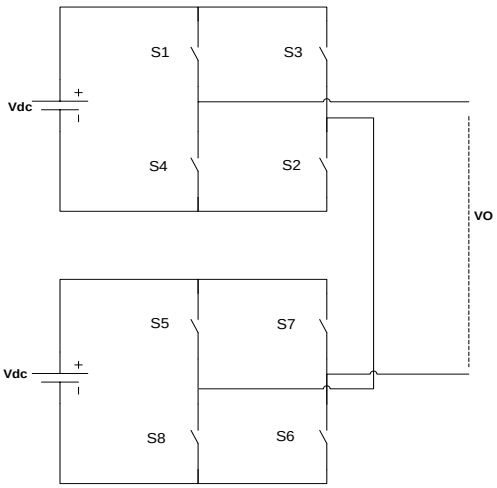

Figure 8. Simulink model of five level inverter

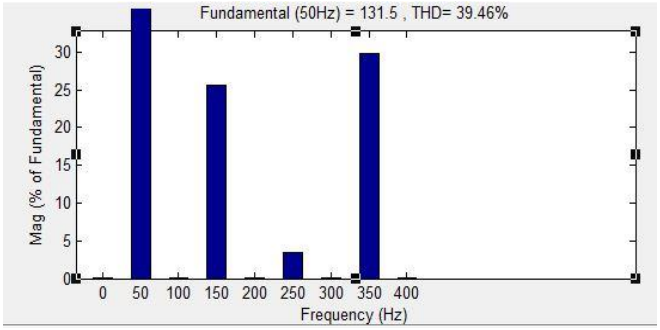

Figure 9. Total harmonic distortion percentage of five level

C. *Seven Level Inverter*

Three H-Bridges are connected with three distinct DC generating units in series in case of seven level inverter. Equal phase method is used to calculate bridges switching angles and fast Fourier transform is used to measure THD. Twelve mosfets are used as a switch with triggering pulses generated by PWM generator in seven level cascaded H-Bridge configuration.

As discussed earlier, triggering pulses are given from PWM generator. Four switches S1, S2, S6 and S10 are used to operates for getting +V while other four switches S3, S7, S11 and S12 are used to operates for -V. Similarly, remaining switches are used for both positive and negative voltages like S9 for 2V, S5 for 3V, S4 for -2V and S8 for getting -3V. Fig 10 shows output waveform of 7 level inverter and THD is 26.78% shown in fig 11.

Phase delays and firing angles given to each switch is shown in table 4.

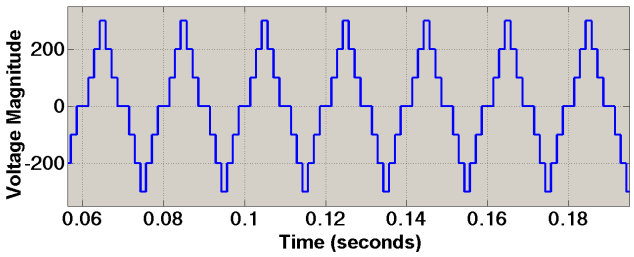

Figure 10. Output waveform of seven level inverter

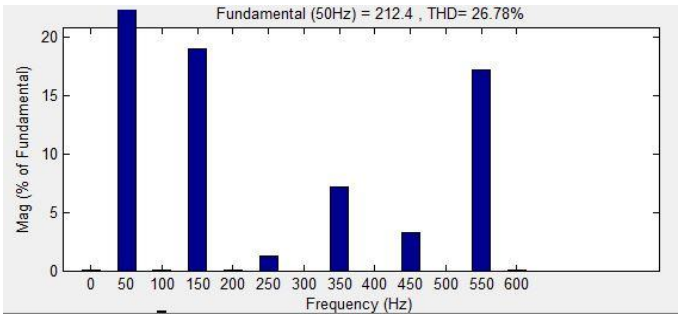

Figure 11. Total harmonic distortion percentage of seven level

TABLE IV. TIMING TABLE OF SEVEN LEVEL INVERTER

Phase	0	V	2V	3V	2V	V	0	-V	-2V	-3V	-2V	-V	0
Switching angles	25.71	51.42	77.14	102.86	128.58	154.29	205.71	231.42	257.14	282.86	308.58	334.29	360
Phase Delay	0.0014	0.0028	0.0042	0.0056	0.0071	0.0085	0.0114	0.0128	0.0142	0.0157	0.0171	0.0185	0.02
S1, S2, S6 & S10		35.70%											
S9			21.42%										
S5				7.14%									
S3,S7, S11&S12								35.70%					
S4									21.452%				
S8										7.14%			

TABLE V. TIMING TABLE OF NINE LEVEL INVERTER

Phase	0	V	2V	3V	4V	3V	2V	V	0	-V	-2V	-3V	-4V	-3V	-2V	-V	0
Switching angles	20	40	60	80	100	120	140	160	200	220	240	260	280	300	320	340	360
Phase delay	0.0011	0.0022	0.0033	0.0044	0.0055	0.0066	0.0077	0.0088	0.0111	0.0122	0.0133	0.0144	0.0155	0.0166	0.0177	0.0188	0.02
S1,S2,S6,S12& S14		38.88%															
S13			27.77%														
S9				16.66%													
S5					5.55												
S3,S7,S11, S15&S16										38.88%							
S4											27.77%						
S8												16.66%					
S12													5.55				

D. Nine Level Inverter

In this type of inverter, 4 H-Bridges connected in series with 4 separate DC generating units. Again, equal phase method is used to calculate switching angles. Fig 12 shows output waveform of nine level. From figure 13, we can see that Total harmonic distortion should be less than the seven-level inverter.

S1, S2, S6 & S14 are closed for positive voltage switches which gives +V, however, other switches are open. Similarly, S3, S7, S11, S15 and S16 are closed for negative cycle which gives –V. Switch 13 is closed for getting 2V. Control of nine level inverter is shown in table 5.

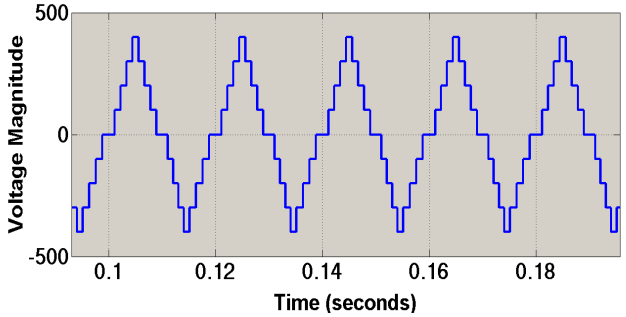

Figure 12. Output waveform of nine level inverter

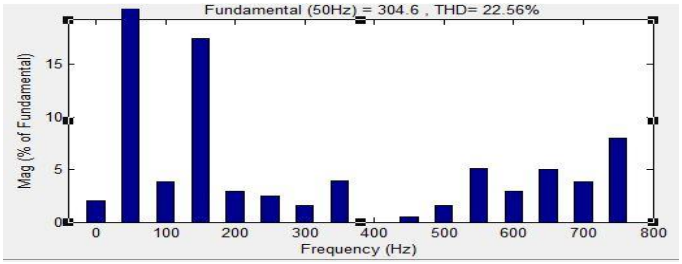

Figure 13. Total harmonic distortion percentage of nine level

TABLE VI. COMPARISON TABLE OF TOTAL HARMONIC DISTORTION

Total Harmonic Distortion percentage comparison of different level of inverter by Equal Phase Method		
S.NO	***Levels of Inverter***	***THD %***
1	3 level	41.42
2	5 level	39.46
3	7 level	26.78
4	9 level	22.56

IV. CONCLUSIONS

In this paper it is concluded that with the increases in the levels of output voltages the output waveform gets smoother and more sinusoidal. It is observed from the above results that with the increase of levels total harmonic distortion reduces.

Total harmonic distortion has inverse relation with number of levels of output voltage as shown in Table VII.

Cascaded H-Bridge configuration is more feasible to implement as compared to ‘diode clamped’ and ‘flying capacitor’ because of few numbers of components and reduced complexity.

Results show that the total harmonic distortion in 3, 5, 7 and 9 level inverters decrease as the number of levels increase. Both Harmonics and dv/dt stresses reduce.

ACKNOWLEDGMENT

I am thankful to the faculty of US Pakistan Center for advanced studies in Energy for guidance and USAID for the support.

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