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Multilevel Inverter Topology having Reduced Number of Input DC Sources and Switches

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***Abstract*—** Multilevel inverters used in medium and high power applications to convert DC power into AC power. We need such inverter which have fewer number of DC sources at input, minimum switching components in the topology and low THD at output voltage waveform. In this paper a single phase 27 level Asymmetrical multilevel inverter (AMLI) topology have presented, The three carrier disposition pulse width modulation (CD-PWM) techniques have used for the proposed 27 level topology, the topology was run in MATLAB/SIMULINK software.

***Keywords*—** Multilevel inverter, total harmonic distortion, pulse width modulation.

I. INTRODUCTION

Initially two level inverters were introduced for conversion of AC into DC, There was too much switching losses, high THD, High voltage stress (dv/dt), low efficiency, need of filter etc. to overcome these problems MLI were designed. MLI gives smoother output waveform than two level inverters. Output voltage of any value and any frequency can be obtained from MLIs. Neutral point clamped (NPC), Flying Capacitor (FC) and Cascaded H-bridge (CHB) are the basic MLI topologies. NPC which is also called diode clamped use clamping diodes to obtain AC current and voltage waveform at output. NPC inverters are available in three output voltage levels, output voltage levels of NPC inverter can increase by adding more clamping diodes to the topology [1]. Flying capacitor inverters have same function of NPC except it uses flying capacitors instead of clamping diodes, extra capacitors are added to FC inverter topology to obtain more voltage levels at output [2]. Cascaded H-bridge inverters use separate multiple blocks to obtain multiple levels at output [3]. Inverters which gives more output levels have smoothers waveform low THD and low losses, but we need more input DC sources and switches to design such inverter topology which increases system losses, cost and complexity. We need such inverter which have reduced number of DC sources and power switches to decrease losses, cost and complexity of the system. Different modulation schemes are used for inverter topologies to obtain approximately sinusoidal waveform. Commonly use modulation techniques are PWM, SVPWM etc. In this paper three popular CD-PWM techniques have used and compare their results with each other, the three techniques give approximately the same results.

II. MODULATION INDEX

Modulation index (MI) is the ratio of magnitude of reference signal with the amplitude of carrier(s) signals [4].

$$\text{Modulation index, MI} = \frac{Vr}{(L-1)Vc} \qquad (1)$$

In this general formula Vr is amplitude of the reference or control signal and Vc is amplitude of the carrier, L is the number of output voltage levels, generally we take sinusoidal as a reference signal and triangular as a carrier, Changing modulation index change the output voltage waveform when modulation index is one we get improved waveform but when we increase or decrease Modulation Index from "1" output voltage waveform distorted, so changing Modulation index give different values of THD.

III. ASYMMETRICAL 17 LEVEL MLITOPOLOGY

The proposed 27 level AMLI topology have "3" input DC sources and "14" switches block diagram of proposed 27 level topology is shown in figure "1" magnitude of input DC sources and equation for output voltage is given in equation "(2)".

$$Vo=V1+V2+V3 \quad (2)$$

Where V1=Vdc, V2=3V1 and V3=9V1

Using equation "(1)" desired output voltage can be obtained.

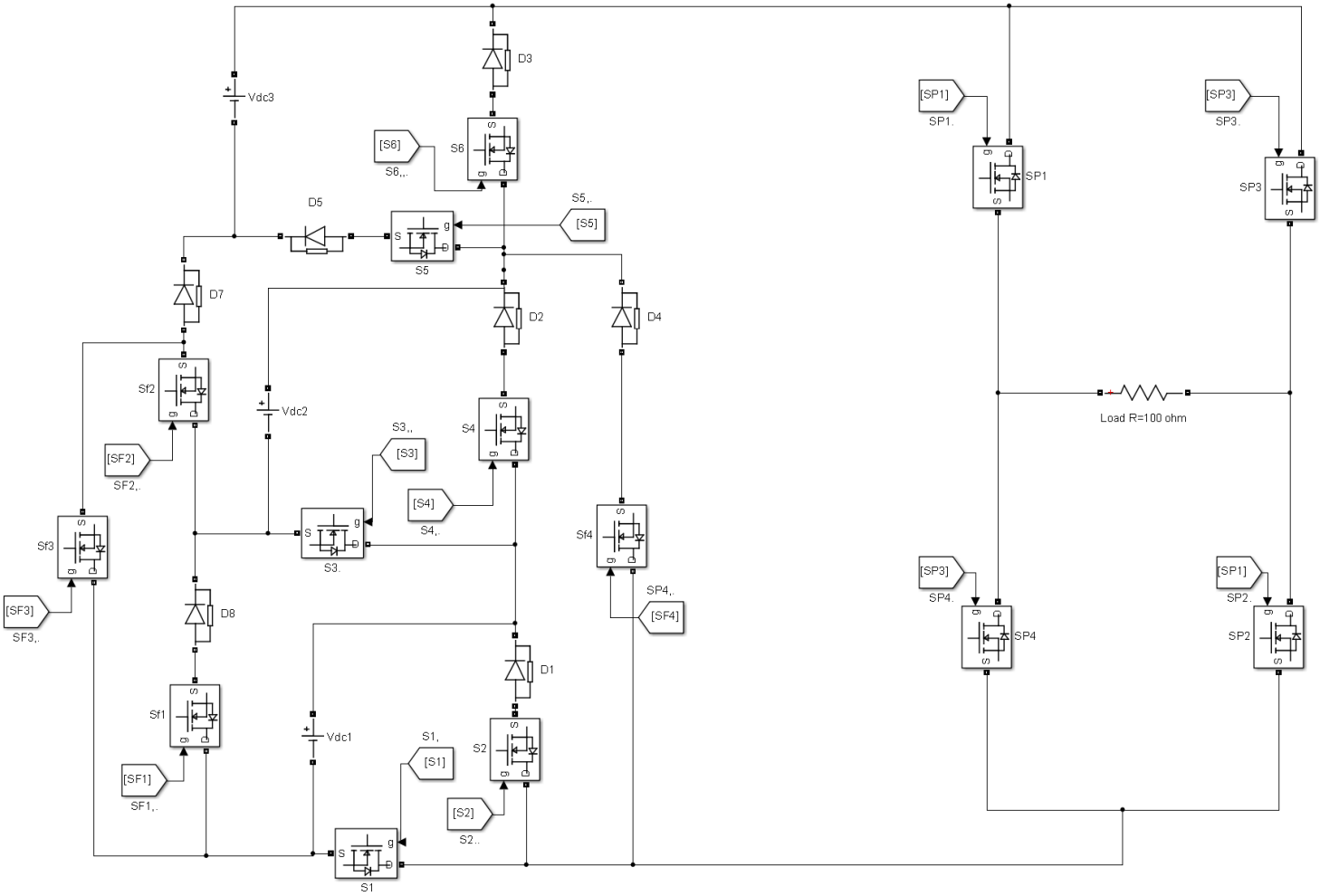

Figure 1: Block diagram of 27 level AMLI topology

For 27 level AMLI topology we need 26 carriers switching status of 14 switches and current flow is given in Table I, current flow in the topology is same for positive and negative half cycles, polarity is only changes by the four switches SP1, SP2, SP3 and SP4. For positive half cycle switches SP1 and SP2 are use while for negative half cycle switches SP3 and SP4 are use.

TABLE I. SWITCHING SEQUENCE OF 27 LEVEL TOPOLOGY.

Output voltage Vo	SP1	SP2	SP3	SP4	S1	S2	S3	S4	S5	S6	SF1	SF2	SF3	SF4	Current flow path
+13V	1	1	0	0	1	0	1	0	1	0	0	0	0	0	Vdc1→ S3→ Vdc2→ S5→ Vdc3→ SP1→ Load R→ SP2→ S1
+12V	1	1	0	0	0	1	1	0	1	0	0	0	0	0	Vdc2→ S5→ Vdc3→ SP1→ Load R→ SP2→S2→ S3
+11V	1	1	0	0	0	1	0	0	1	0	1	0	0	0	Vdc1→ SF1→ Vdc2→ S5→ Vdc3→ SP1→ Load R→ SP2→ S2
+10V	1	1	0	0	1	0	0	1	1	0	0	0	0	0	Vdc1→ S4→S5→ Vdc3→ SP1→ Load R→ SP2→ S1
+9V	1	1	0	0	0	1	0	1	1	0	0	0	0	0	Vdc3→ SP1→ Load R→ SP2→S2→S4→S5
+8V	1	1	0	0	0	1	0	0	0	0	0	0	1	0	Vdc1→SF3→Vdc3→SP1→LoadR→SP2→S2
+7V	1	1	0	0	1	0	0	1	0	0	0	1	0	0	Vdc1→S4→Vdc2→SF2→Vdc3→ SP1→ Load R→SP2→S1
+6V	1	1	0	0	0	0	0	0	0	0	0	1	0	1	Vdc2→ SF2→Vdc3→SP1→ Load R→ SP2→ SF4
+5V	1	1	0	0	0	0	1	0	0	0	0	0	1	1	Vdc2→ S3→Vdc1→SF3 →Vdc3→ SP1→ Load R→ SP2→ SF4
+4V	1	1	0	0	1	0	1	0	0	1	0	0	0	0	Vdc1→ S3→ Vdc2→ S6→ SP1→ Load R→ SP2→ S1
+3V	1	1	0	0	0	1	1	0	0	1	0	0	0	0	Vdc2→ S6→SP1→ Load R→ SP2→ S2→ S3
+2V	1	1	0	0	0	1	0	0	0	1	1	0	0	0	Vdc1→ SF1→Vdc2→S6→SP1→ Load R→ SP2→ S2
+1V	1	1	0	0	1	0	0	1	0	1	0	0	0	0	Vdc1→S4→S6→SP1→Load R→ SP2→ S1
0V	1	0	1	0	1	0	0	1	0	1	0	0	0	0	No flow of current
-1V	0	0	1	1	1	0	0	1	0	1	0	0	0	0	Vdc1→S4→S6→SP3→Load R→ SP4→ S1
-2V	0	0	1	1	0	1	0	0	0	1	1	0	0	0	Vdc1→SF1→Vdc2→S6→SP3→ Load R→ SP4→ S2
-3V	0	0	1	1	0	1	1	0	0	1	0	0	0	0	Vdc2→ S6→SP3→ Load R→ SP4→ S2→ S3
-4V	0	0	1	1	1	0	1	0	0	1	0	0	0	0	Vdc1→ S3→ Vdc2→ S6→ SP3→ Load R→ SP4→ S1
-5V	0	0	1	1	0	0	1	0	0	0	0	0	1	1	Vdc2→ S3→Vdc1→SF3 →Vdc3→ SP3→ Load R→ SP4→ SF4
-6V	0	0	1	1	0	0	0	0	0	0	0	1	0	1	Vdc2→ SF2→Vdc3→SP3→ Load R→ SP4→ SF4
-7V	0	0	1	1	1	0	0	1	0	0	0	1	0	0	Vdc1→ S4→Vdc2→SF2 →Vdc3→ SP3→ Load R→ SP4→ S1
-8V	0	0	1	1	0	1	0	0	0	0	0	0	1	0	Vdc1→ SF3→ Vdc3→SP3→ Load R→ SP4→ S2
-9V	0	0	1	1	0	1	0	1	1	0	0	0	0	0	Vdc3→ SP3→ Load R→ SP4→S2→ S4→ S5
-10V	0	0	1	1	1	0	0	1	1	0	0	0	0	0	Vdc1→ S4→S5→ Vdc3→ SP3→ Load R→ SP4→ S1
-11V	0	0	1	1	0	1	0	0	1	0	1	0	0	0	Vdc1→ SF1→ Vdc2→ S5→ Vdc3→ SP3→ Load R→ SP4→ S2
-12V	0	0	1	1	0	1	1	0	1	0	0	0	0	0	Vdc2→ S5→ Vdc3→ SP3→ Load R→ SP4→S2→ S3
-13V	0	0	1	1	1	0	1	0	1	0	0	0	0	0	Vdc1→ S3→ Vdc2→ S5→ Vdc3→ SP3→ Load R→ SP4→ S1

For 27 level topology "26" carriers are given in Table "II(A)" and Table "II(B)" "13" carriers are for positive half cycle while "13" carriers are for negative half cycle ,for zero level of output voltage we don't need any carrier

TABLE II. (A): BINARY REPRESENTATION OF PULSE PATTERN FOR 24 CARRIERS.

Output voltage Vo	**P1**	**P2**	**P3**	**P4**	**P5**	**P6**	**P7**	**P8**	**P9**	**P10**	**P11**	**P12**	**P13**
0V	0	0	0	0	0	0	0	0	0	0	0	0	0
+1V	1	0	0	0	0	0	0	0	0	0	0	0	0
+2V	1	1	0	0	0	0	0	0	0	0	0	0	0
+3V	1	1	1	0	0	0	0	0	0	0	0	0	0
+4V	1	1	1	1	0	0	0	0	0	0	0	0	0
+5V	1	1	1	1	1	0	0	0	0	0	0	0	0
+6V	1	1	1	1	1	1	0	0	0	0	0	0	0
+7V	1	1	1	1	1	1	1	0	0	0	0	0	0
+8V	1	1	1	1	1	1	1	1	0	0	0	0	0
+9V	1	1	1	1	1	1	1	1	1	0	0	0	0
+10V	1	1	1	1	1	1	1	1	1	1	0	0	0
+11V	1	1	1	1	1	1	1	1	1	1	1	0	0
+12V	1	1	1	1	1	1	1	1	1	1	1	1	0
+13V	1	1	1	1	1	1	1	1	1	1	1	1	1
+13V	1	1	1	1	1	1	1	1	1	1	1	1	1
+12V	1	1	1	1	1	1	1	1	1	1	1	1	0
+11V	1	1	1	1	1	1	1	1	1	1	1	0	0
+10V	1	1	1	1	1	1	1	1	1	1	0	0	0
+9V	1	1	1	1	1	1	1	1	1	0	0	0	0
+8V	1	1	1	1	1	1	1	1	0	0	0	0	0
+7V	1	1	1	1	1	1	1	0	0	0	0	0	0
+6V	1	1	1	1	1	1	0	0	0	0	0	0	0
+5V	1	1	1	1	1	0	0	0	0	0	0	0	0
+4V	1	1	1	1	0	0	0	0	0	0	0	0	0
+3V	1	1	1	0	0	0	0	0	0	0	0	0	0
+2V	1	1	0	0	0	0	0	0	0	0	0	0	0
+V	1	0	0	0	0	0	0	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE III. TABLE II (B): BINARY REPRESENTATION OF PULSE PATTERN FOR "24" CARRIERS.

Output voltage Vo	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13
0V	0	0	0	0	0	0	0	0	0	0	0	0	0
-1V	1	0	0	0	0	0	0	0	0	0	0	0	0
-2V	1	1	0	0	0	0	0	0	0	0	0	0	0
-3V	1	1	1	0	0	0	0	0	0	0	0	0	0
-4V	1	1	1	1	0	0	0	0	0	0	0	0	0
-5V	1	1	1	1	1	0	0	0	0	0	0	0	0

-6V	1	1	1	1	1	1	0	0	0	0	0	0	0
-7V	1	1	1	1	1	1	1	0	0	0	0	0	0
-8V	1	1	1	1	1	1	1	1	0	0	0	0	0
-9V	1	1	1	1	1	1	1	1	1	0	0	0	0
-10V	1	1	1	1	1	1	1	1	1	1	0	0	0
-11V	1	1	1	1	1	1	1	1	1	1	1	0	0
-12V	1	1	1	1	1	1	1	1	1	1	1	1	0
-13V	1	1	1	1	1	1	1	1	1	1	1	1	1
-13V	1	1	1	1	1	1	1	1	1	1	1	1	1
-12V	1	1	1	1	1	1	1	1	1	1	1	1	0
-11V	1	1	1	1	1	1	1	1	1	1	1	0	0
-10V	1	1	1	1	1	1	1	1	1	1	0	0	0
-9V	1	1	1	1	1	1	1	1	1	0	0	0	0
-8V	1	1	1	1	1	1	1	1	0	0	0	0	0
-7V	1	1	1	1	1	1	1	0	0	0	0	0	0
-6V	1	1	1	1	1	1	0	0	0	0	0	0	0
-5V	1	1	1	1	1	0	0	0	0	0	0	0	0
-4V	1	1	1	1	0	0	0	0	0	0	0	0	0
-3V	1	1	1	0	0	0	0	0	0	0	0	0	0
-2V	1	1	0	0	0	0	0	0	0	0	0	0	0
-V	1	0	0	0	0	0	0	0	0	0	0	0	0
0V	0	0	0	0	0	0	0	0	0	0	0	0	0

For generation of positive half cycle of voltage we need only positive carriers and for negative half cycle we need only negative carriers. In positive half cycle value of each negative carrier is “0” similarly in negative half cycle value of each positive carrier is “0” so in Table II(A) and Table II(B) we not mention the value of negative carriers for positive half cycle and value of positive carriers for negative half cycle.

IV. Modulation Techniques for 27 Levels Topologies

Three CD-PWM techniques have used for the 27 level AMLI topology, for 27 levels we need “26” carriers, waveform of the three modulation techniques is shown in figures 2, 3 and 4.

A. PD-PWM scheme

In simple PD-PWM technique all carriers are in phase, have same amplitude and frequency. Waveform of PD-PWM technique is given in figure 2 for “26’ carriers.

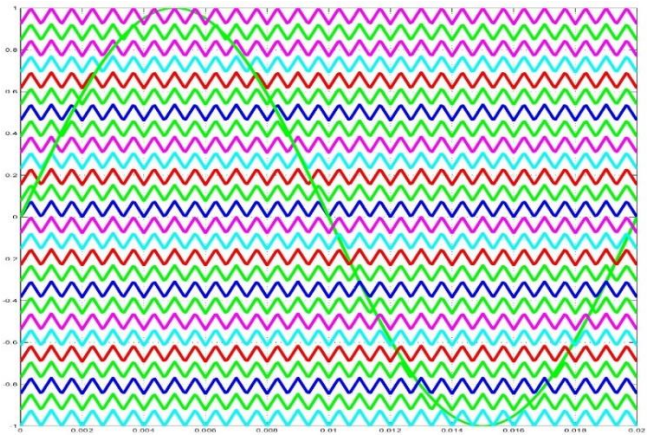

Figure 2: Phase Disposition-PWM

In this figure each carrier have frequency of 1.5 kHz the control signal is a sine signal of frequency 50 Hz.

B. POD-PWM scheme

In simple POD-PWM technique carriers are divided into positive and negative sets all carriers have same amplitude and frequency but set of negative carriers are 180 degree out of phase from set of positive carriers and vice versa. Waveform of POD-PWM technique at carrier's frequency of 1.5 kHz and control signal of 50 Hz is given in figure 3 for "26' carriers.

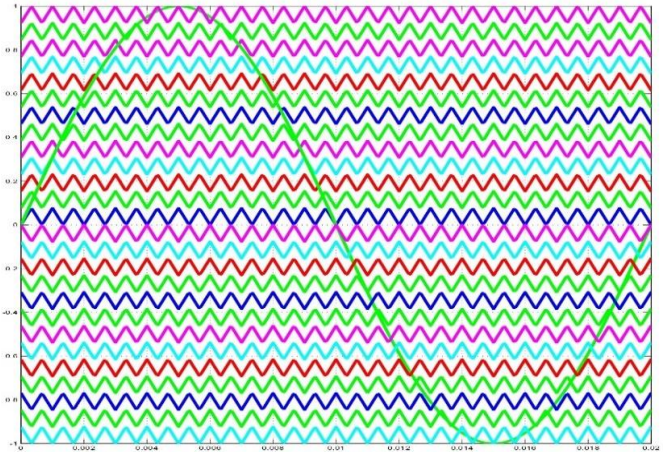

Figure 3: Phase Opposition Disposition-PWM

C. APOD-PWM scheme

In simple APOD-PWM technique all carriers have same amplitude and frequency neighbor carriers of each carrier are 180 degree out of phase, Waveform of APOD-PWM technique is given in figure 4 for "26" carriers.

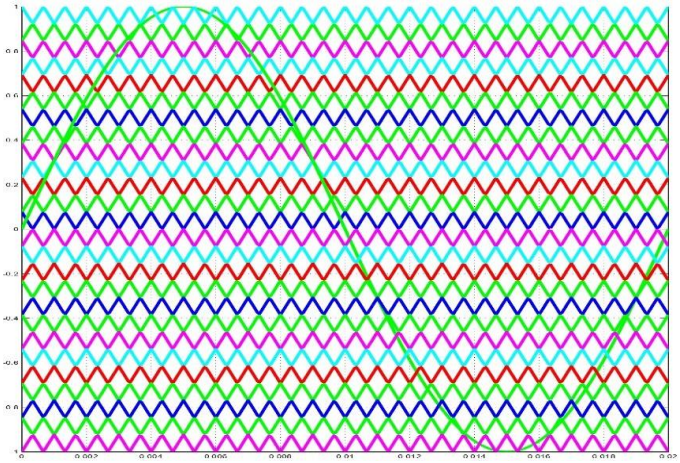

Figure 4: Alternate Phase Opposition Disposition-PWM

In this figure each carrier have frequency of 1.5 kHz reference signal is a sinusoidal signal of frequency 50 Hz.

V. Logic Gates Combination and Equation for Input Signal to Each Switch

In the proposed 27 levels AMLI topology four logic gates SP1, SP2, SP3 and SP4 have used for polarity, switches SP1 and SP2 used for positive half cycle while switches SP3 and SP4 used for negative half cycle for output voltage waveform.

Logical equations are obtained from Table II (A) and Table II (B) for each switch

- Logical equation and combination of logic gates for switches SP2 and SP3.

SP2= P1 (3)

SP4=N1 (4)

Switches SP2 and SP4 are directly connected to P1 and N1 respectively.

Switches SP2 and SP4 are directly connect to the relational operator of carriers P1 and N1 respectively.

- Logical equation and combination of logic gates for switch SP1.

$SP1= (\overline{P1} \bullet \overline{N1})+N1$ (5)

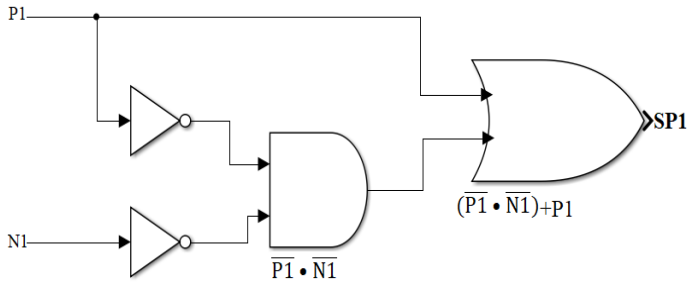

Figure 5: Representation of logic gates for switch SP1

- Logical equation and combination of logic gates for switch SP3.

$SP3= (\overline{P1} \bullet \overline{N1})+N1$ (6)

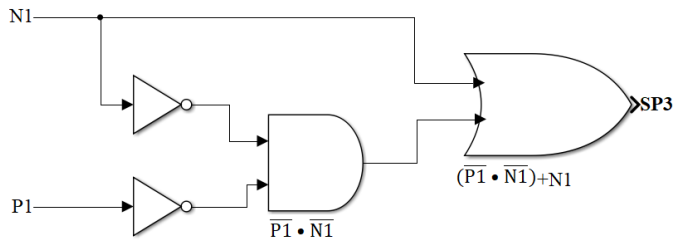

Figure 6: Representation of logic gates for switch SP3

- Logical equation and combination of logic gates for switch S1.

$$S1=(P1 \oplus P2) + (P4 \oplus P5) + (P7 \oplus P8)+(P10 \oplus P11)+(N1 \oplus N2) + (N4 \oplus N5) + (N7 \oplus N8) + (N10 \oplus N11)+(\overline{P1} \bullet \overline{N1}) + P13 + N13 \quad (7)$$

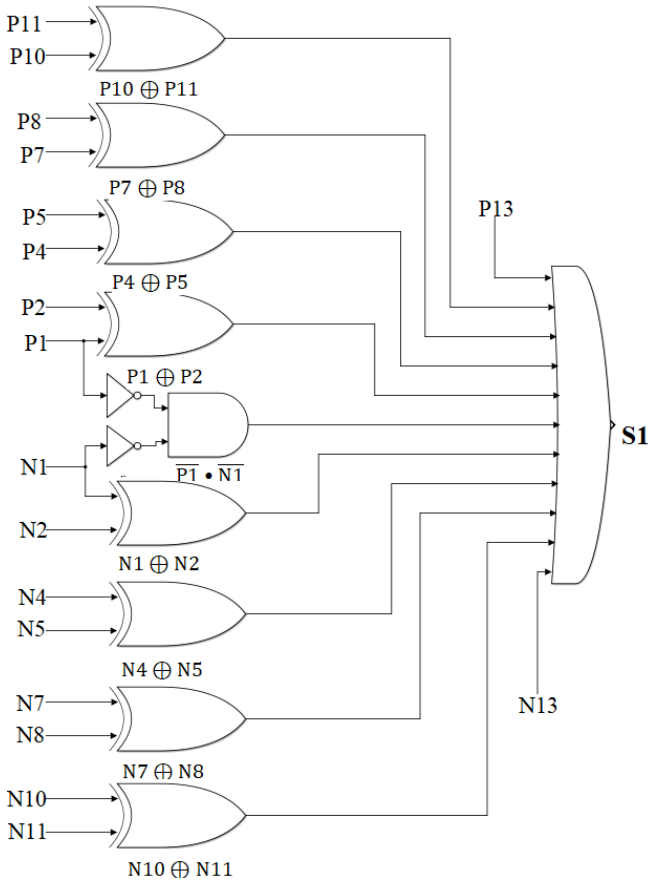

Figure 7: Representation of logic gates for switch S1

- Logical equation and combination of logic gates for switch S2.

$$S2=(P2 \oplus P4) + (P8 \oplus P10) + (P11 \oplus P13)+(N2 \oplus N4) + (N8 \oplus N10) + (N11 \oplus N13) \quad (8)$$

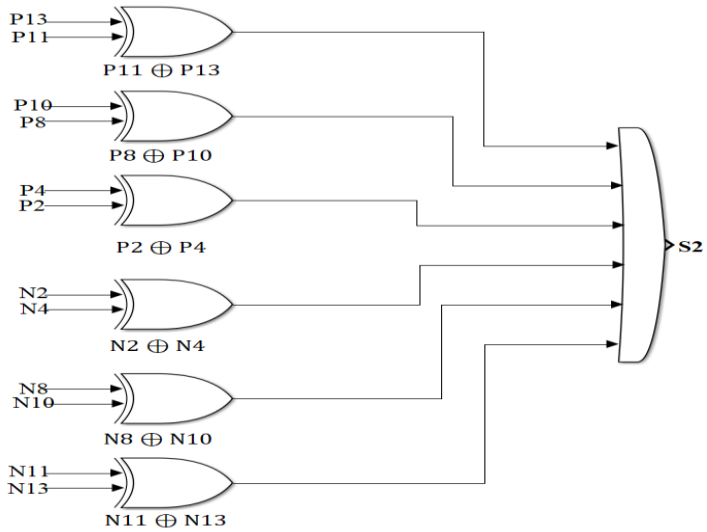

Figure 8: Representation of logic gates for switch S2

- Logical equation and combination of logic gates for switch S3.

$$S3=(P3 \oplus P6) + P12 + (N3 \oplus N6) + N12 \quad (9)$$

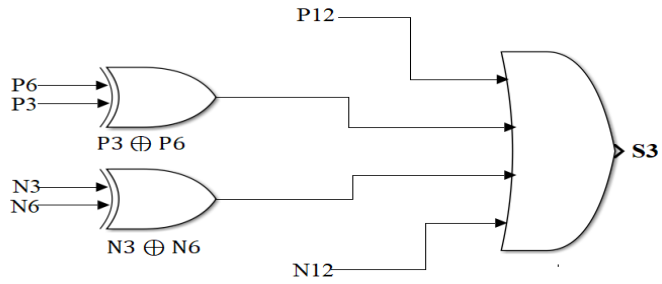

Figure 9: Representation of logic gates for switch S3

- Logical equation and combination of logic gates for switch S4.

$$S4=(P1 \oplus P2) + (P7 \oplus P8) + (P9 \oplus P11)+(N1 \oplus N2) + (N7 \oplus N8) + (N9 \oplus N11) + (\overline{P1} \bullet \overline{N1}) \quad (10)$$

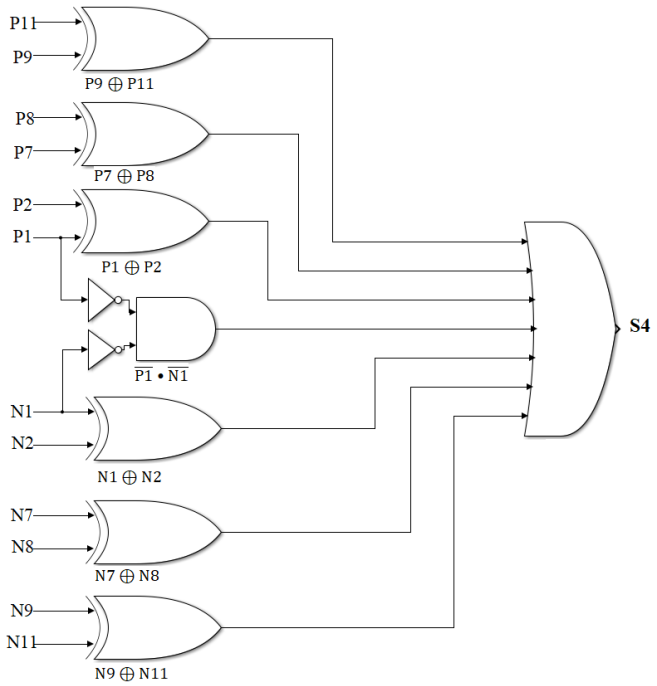

Figure 10: Representation of logic gates for switch S4

- Logical equation and combination of logic gates for switch S5.

S5= P9+N9 (11)

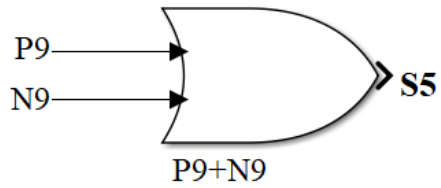

Figure 11: Representation of logic gates for switch S5

- Logical equation and combination of logic gates for switch S6.

$S6=(P1 \oplus P5)+(N1 \oplus N5) + (\overline{P1} \bullet \overline{N1})$ (12)

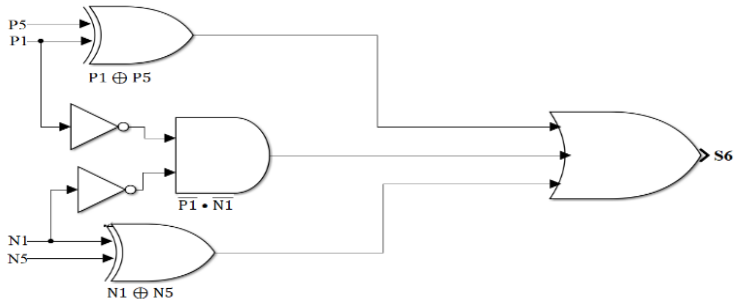

Figure 12: Representation of logic gates for switch S6

- Logical equation and combination of logic gates for switch SF1.

$SF1=(P2 \oplus P3) + (P11 \oplus P12)+(N2 \oplus N3) + (N11 \oplus N12)$ (13)

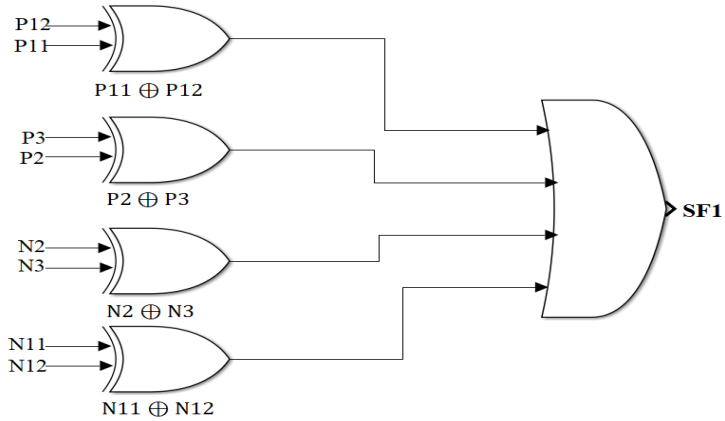

Figure 13: Representation of logic gates for switch SF1

- Logical equation and combination of logic gates for switch SF2.

$SF2=(P6 \oplus P8) + (N6 \oplus N8)$ (14)

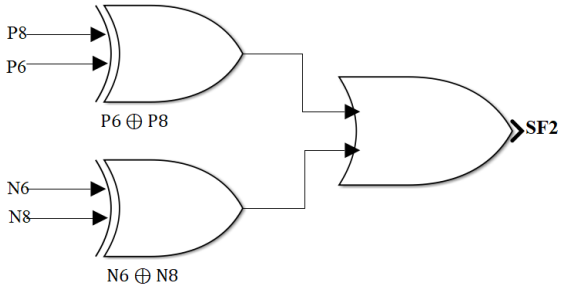

Figure 14: Representation of logic gates for switch SF2

- Logical equation and combination of logic gates for switch SF3.

$$SF3=(P5 \oplus P6) + (P8 \oplus P9)+(N5 \oplus N6) + (N8 \oplus N9) \quad (15)$$

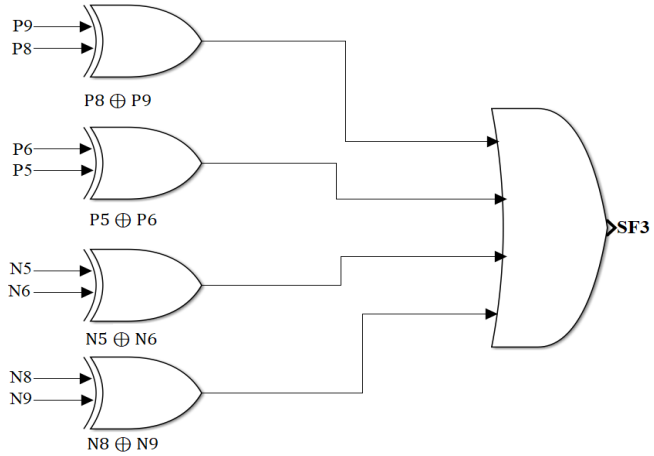

Figure 15: Representation of logic gates for switch SF3

- Logical equation and combination of logic gates for switch SF4.

$$SF4=(P5 \oplus P7) + (N5 \oplus N7) \quad (16)$$

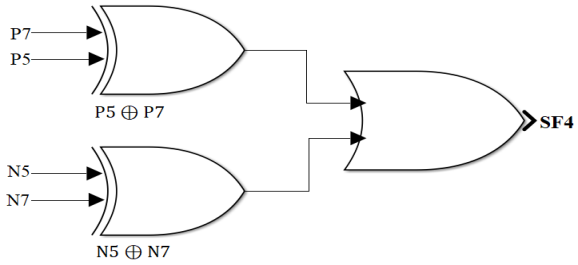

Figure 16: Representation of logic gates for switch SF4

VI. Simulation Results

The proposed 27 level topology was run in MATLAB/SIMULINK software, control signal was taken a pure sinusoidal of 50 Hz frequency, carriers of 1.5 kHz frequency, load resistance of 100 ohm, voltage of three DC sources Vdc1, Vdc2 and Vdc3 were taken 220/13V, 3×220/13V and 9×220/13V respectively . Modulation index was change from 0.1 To 1.5 THD against each CD-PWM technique at different Modulation Indexes is given in Table III.

TABLE IV. THD VS MODULATION INDEX AT 1.5 KHZ FREQUENCY

MI at 1.5 kHz	THD (in percentage)		
	PD-PWM	POD-PWM	APOD-PWM
0.1	43.89	44.34	43.32
0.2	24.63	24.63	24.79
0.3	15.27	14.56	14.79
0.4	10.66	11.34	10.82
0.5	9.23	8.10	9.19
0.6	7.81	7.46	7.67
0.7	6.23	5.65	5.75
0.8	5.53	5.40	4.84
0.9	5.17	5.32	5.34
1	4.48	4.69	4.53
1.1	5.04	5.08	4.49
1.2	7.74	7.74	8.29
1.3	10.67	10.80	10.39
1.4	13.14	13.00	13.25
1.5	15.33	15.21	15.74

In Table III PD-PWM, POD-PWM and APOD-PWM gives improved results of THD 4.48, 4.69 and 4.53 at MI of 1 respectively, APOD-PWM gives more improved result at MI of 1.1 but there is little difference between THD of 4.53 and 4.49 also in over modulation we need extra control strategies so we have to choose THD of 4.53 at MI of 1 to avoid any complexity and inconvenience. Graph of each Modulation technique is drawn in figures 17, 18 and 19 and in figure 20 combine graph is drawn to compare the results of the three CD-PWM techniques.

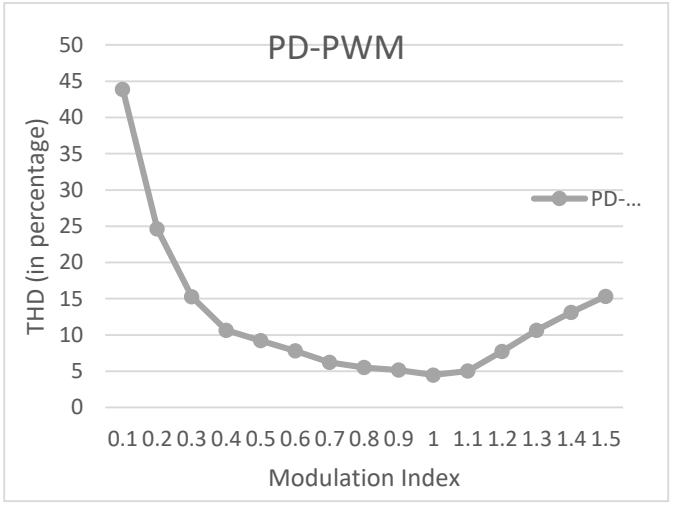

Figure 17: THD at different Modulation Indexes (PD-PWM)

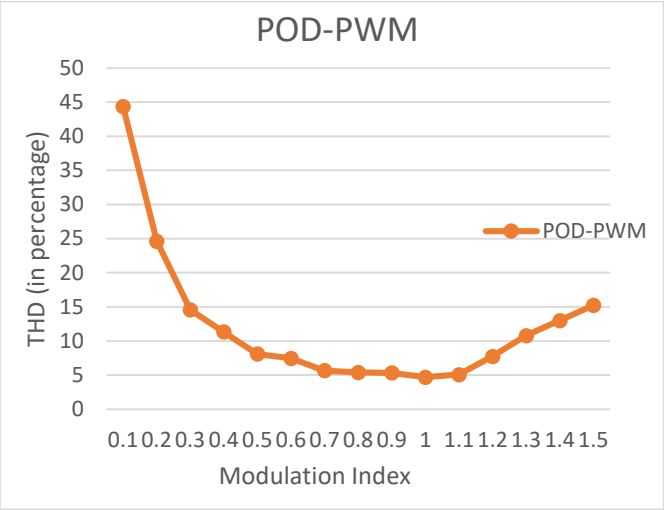

Figure 18: THD at different Modulation Indexes (POD-PWM)

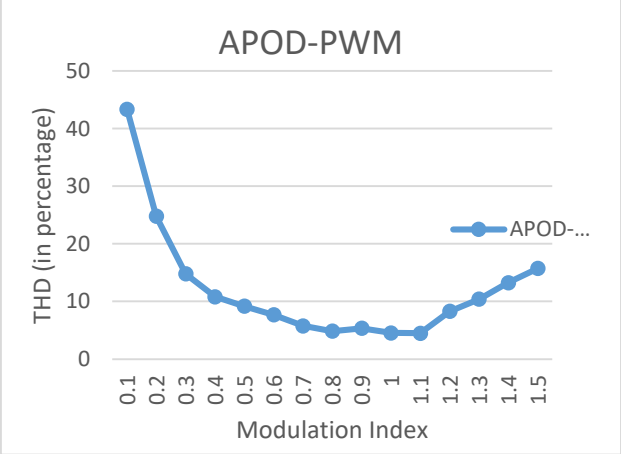

Figure 19: THD at different Modulation Indexes (APOD-PWM)

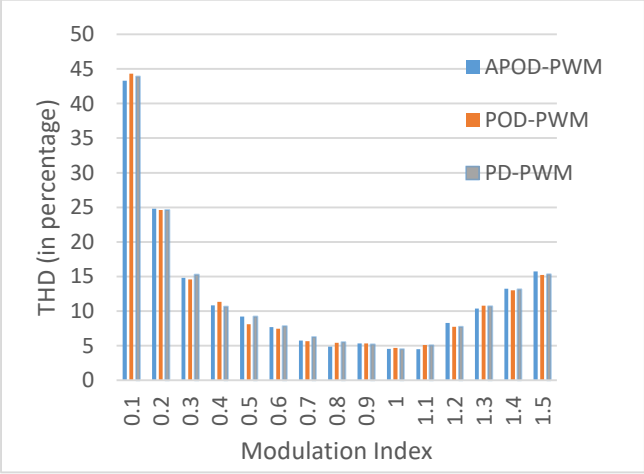

Figure 20: Comparative graph of all CD-PWM techniques

The three graphs in figure 17,18 and 19 show that as Modulation index increase or decrease from 1 THD increases, only in figure 19 of APOD-PWM we have minimum THD at 1.1 but when we further increase value of MI THD increases.

Combined graph of the three Modulation techniques in Figure 20 show that all CD-PWM techniques have approximately the same result.

From Table III FFT analysis of each CD-PWM technique is given in figures 21 to 26.

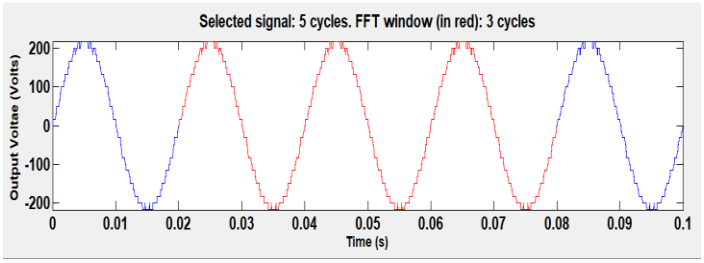

Figure 21: output voltage waveform of PD-PWM at R=100 ohm and MI=1

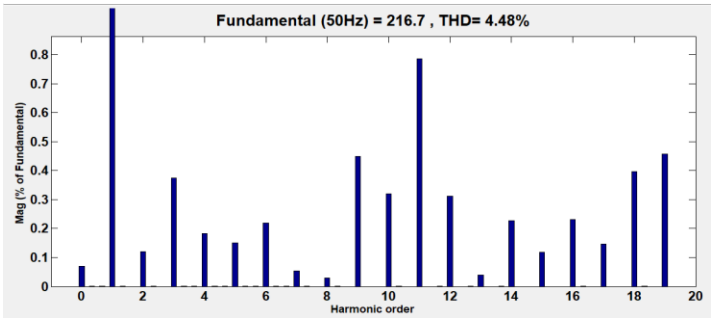

Figure 22: FFT of PD-PWM scheme (R=100 ohm and MI=1)

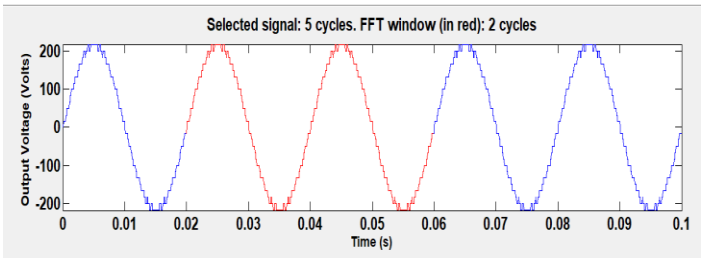

Figure 23: output voltage waveform of POD-PWM at R=100 ohm and MI=1

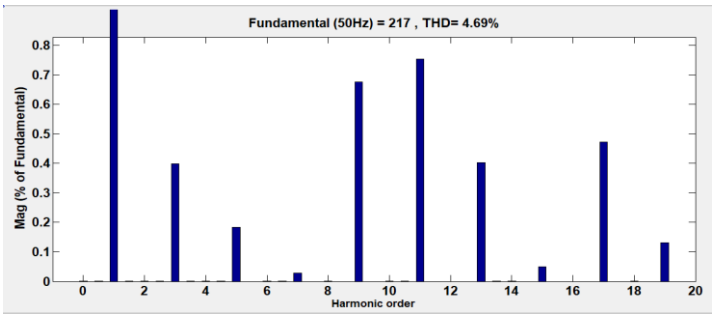

Figure 24: FFT of POD-PWM scheme (R=100 ohm and MI=1)

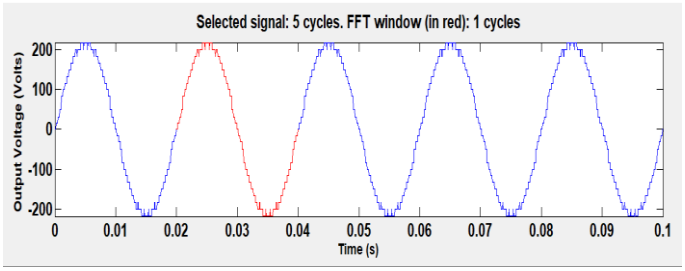

Figure 25: output voltage waveform of APOD-PWM at R=100 ohm and MI=1

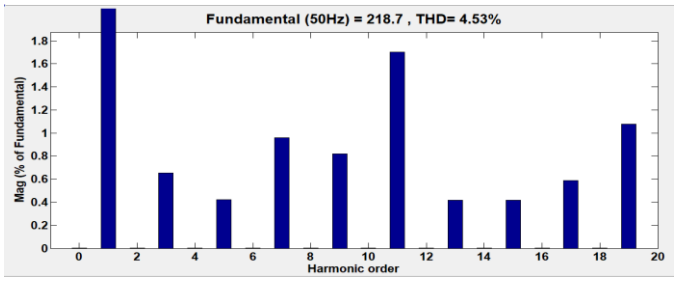

Figure 26: FFT of APOD-PWM scheme (R=100 ohm and MI=1)

VII. Comparison of Proposed 27 Levels AMLI Topology With Others Topologies

27 level AMLI topology was compared in Table IV with few other topologies to show that the proposed 27 level AMLI topology have reduced number of input DC sources and switches. In table "L" represent the numer of output voltage levels.

TABLE V. COMPARISON OF PROPOSED 27 LEVEL AMLI TOPOLOGY WITH OTHER TOPOLOGIES

Inverter topology	**Output levels L**	**DC sources**	**Capacitors**	**Switches**
Proposed 27 level	27	3	0	14
NPC [5]	L	1	L-1	2× (L-1)
FC[5]	L	1	L-1	2× (L-1)
CHB[5]	L	12	(L-1)/2	2× (L-1)
[6]	25	6	6	21
[7]	15	7		16
[8]	15	3		12
[9]	25	6	6	30
[10]	21	3	3	14
[11]	25	12		16
[12]	25	12		26

From Table IV we concluded that the proposed 27 level inverter topology have reduced number of input DC sources and switches.

Conclusion and Future Work

In this paper 27 level AMLI topology was presented and run in MATLAB/SIMULINK software. Three CD-PWM techniques were used the three modulation schemes give approximately same THD which is less than 5%, according to IEEE standard 519, 5% value of THD with filter and 15% to 25% without filter is allowed [13]. The proposed 27 level AMLI topology gives THD of less than 5% without a filter. The proposed topology was compared with conventional and few other topologies and was found that the proposed 27 level AMLI topology have reduced number of input DC sources and switches.

Proposed topology can be extended to 3 phase it can also be practiced for solar and wind power.

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