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Temperature and Channel width Dependence of Novel Lateral Gate VJFET

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***Abstract*—**2D numerical simulation of normally off vertical N-channel JFET with novel internal lateral gate configuration designed on a 9.4 µm, 7 × 1015 cm−3 doped drift layer is presented. The study covers an interval of blocking voltages ranging from 600 V to 933 V for various temperatures and channel widths. The effect of elimination of vertical JFET gates and variation in channel width on the on-state/breakdown performance is carefully investigated. The device performance has been compared in terms of blocking voltages, specific on-state resistance and maximum output current density in the temperature range from room temperature up to 473 K. Normally-off operation with blocking voltage (Vbl) of 933 V is demonstrated for a gate voltage of -20 V. The goal of this work is to predict the performance of lateral gate VJFET configuration and have a deep insight into the relationship between the device's electrical/thermal characteristics and channel thickness. The detailed investigation reveals that lateral gate configuration offers less resistance to leakage current reducing the blocking capability of the device. Though, it's excellent on state performance in terms of high saturation current (1.23A) and low on-resistance (3.6 m Ω) makes this VJFET an excellent device for fast power switching applications.

***Keywords*—** VJFET, channel width, Normally-off, Transconductance, on-resistance

I. INTRODUCTION

Power electronics has seen replacement of Si and GaAs with wide-band-gap semiconductors as the recent progress and development has caused Si semiconductor technology to approach certain theoretical material's limitations [1-2]. In many power device applications, silicon has proved unsuitable because Si based power devices have failed to meet some advanced technological needs including higher blocking voltage, switching frequency, efficiency, and reliability. Today, the focus of research is to discover the new semiconductor materials for power device applications to meet the advanced technological needs. Recently, the wide-band-gap semiconductors such as SiC, GaN, and ZnSe have received remarkable attention as promising semiconductor compounds for their high temperature, high frequency, and high power device applications due to their high thermal conductivity, high critical field for breakdown and resistance to chemical attack [3-5]. Particularly SiC has been recognized as a superior semiconductor for high-power and high temperature applications in view of its wide band gap, large avalanche breakdown field, excellent thermal conductivity, and high electron saturation drift velocity . SiC is resistant to chemical

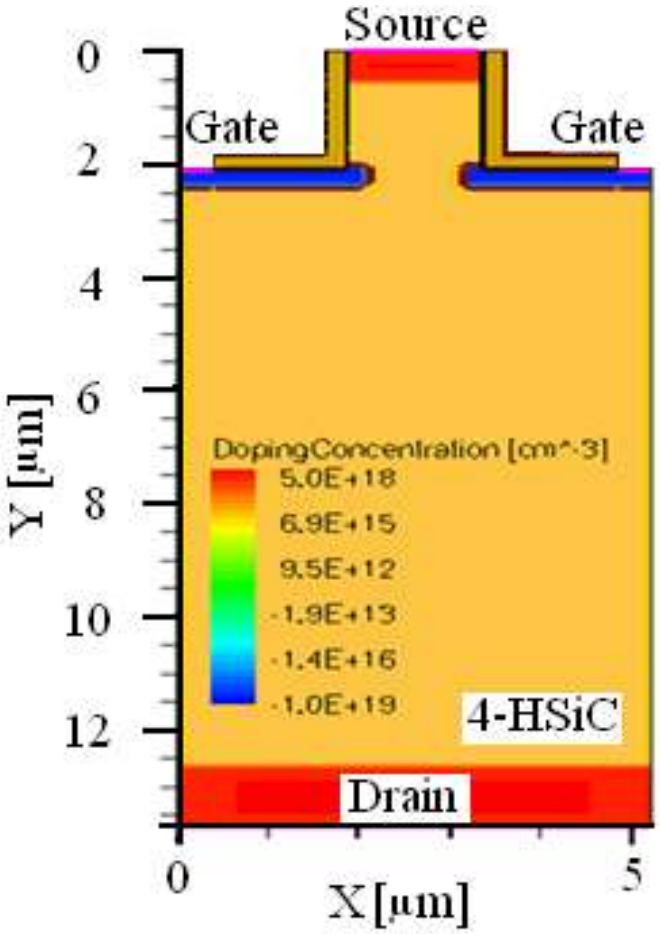

Figure 1. Cross-sectional view of simulated VJFET.

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attack and radiation damage because of its large Si-C bonding energy ensures its stability at even high temperatures. These desirable characteristics make SiC a material of choice for efficient high power, high temperature, high voltage and high frequency device applications, due to the favorable combination of transport parameters [6-9].

Several types of SiC–based transistors have been proposed and being developed. JFETs and BJTs are identified as remarkable switching candidates. JFET is a uni-polar device and so is forgiving with respect to material quality. SiC JFETs offer low on-resistance and high stability in harsh ambient conditions. They don't have to suffer from bipolar instability. The JFETs require comparably high negative gate voltages while the BJTs require a considerable base current. For a three-phase power electronic inverter used in hybrid electric vehicles (HEVs), the power would be 50 KW approximately and the switching frequency approximately 10 KHz [10-11]. In such applications the main reason to use a SiC switch would not be the high switching speed, but more likely the low forward voltage drop and high thermal stability.

Recently, 4H-SiC based 10 KV-class MOSFETs [12-13] and IGBTs [1] have been described. These MOS-based devices inherently suffer from low channel mobility, low threshold-voltage and high temperature instability due to native oxide. [14]. JFETs, being the most mature switching candidates in SiC semiconductor technology, have several advantages over MOSFET and other switching devices. Owing to its wide band gap (~3.26 eV), SiC based JFETs exhibit high temperature stability making normally-off designs possible due to the high value of the built-in voltage. JFETs use reverse biased p-n junction as a current controlling mechanism and can therefore reliably operate as high-temperature gate-voltage-controlled switches eliminating the requirement of a high quality SiO2/SiC interface as needed in the MOSFET. The SiC MOSFET would be the device of choice as soon as the SiO2/SiC interface and reliability issues are resolved. SiC JFETs with lateral and vertical type structures have been developed [15-18]. Their structures exhibit the normally–on characteristics, but recently the devices with normally-off behavior have also been developed. In Normally off JFETs, a narrow and relatively low doped channel is required to ensure the N-off operation. Normally off VJFET devices allow reliable operation and are desirable for fail-safe protection [19]. SiC JFETs discussed in this paper are normally-off vertical type devices with lateral gates on channel shoulders, designed and simulated using Sentaurus TCAD [20].

II. DEVICE STRUCTURE

The important design parameters should be considered carefully while defining a device structure, as the choice of parameters directly influence the performance in view of a JFET's saturation current, on-resistance and blocking capability. The device structure was defined in Sentaurus structure editor [20]; a cross-sectional view is shown schematically in Fig. 1. The active device area is similar to one presented by J. H. Zhao et al. [21] with major structural variations at channel region by vertical gate elimination where P + buried layers act as gates.

The device has an n– vertical channel and drift region with a doping concentration of 7.0×1015 cm-3 and the p++ lateral gate regions created on the shoulders of n-channel intruding in drift region. The n++ drain and source regions are doped with a concentration of 5.0×1018 cm-3. The SiO2 is used as a passivation layer providing an insulation to protect surface properties of the device. The channel width varies between 1.25 to 1.45 μm, while the blocking layer is designed to have a thickness of approximately 9.4 μm.

III. SIMULATION MODELS

Besides providing a deep insight, especially for aggressively scaled devices, for which complex physical phenomena and small dimensions severely limit the descriptive capabilities of measurements, TCAD simulations exhibit a remarkable prediction upon calibration to proper experimental data. The generation of predictive models play a crucial role in reducing development cycle times and costs in semiconductor industry. This role is highlighted by the 2005 edition of the ITRS, where TCAD is indicated as a crucial enabling methodology supporting the current technological progress.

Simulations rely on physical models and model parameters. To perform reliable and predictive simulations, proper physical models and model parameters are crucial. Models describe the operational phenomena while the model parameters are calibrated to the procedures and materials used to fabricate the devices. The physical models were used for doping dependent mobility with high field saturation effects, impact ionization (Okuto–Crowell model), doping dependent and temperature dependent Shockley-Read-Hall (SRH) recombination and Auger recombination, while the model parameters were compiled for the 4H-SiC polytype as discussed elsewhere [22]. Sentaurus Device also accounts for the anisotropic properties such as anisotropic mobility and anisotropic impact ionization resulting from the hexagonal crystal structure of 4H-SiC.

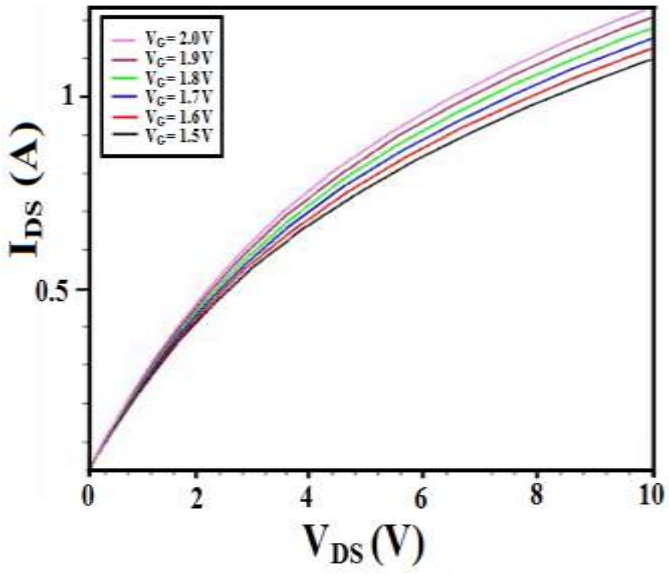

Figure 2. Forward IDS-VDS characteristics curves for different gate voltages.

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IV. SIMULATION RESULTS

The device's forward and blocking characteristics were calibrated for a range of temperatures at different channel widths. It was observed that the channel width and lateral gate configuration have a direct influence on the IV characteristics for a given value of temperature as shown in the Fig. 2. Lateral buried gates offer less resistance to current flow producing high saturation current of 1.23 A with extremely low on-resistance of value 3.6mΩ compared to their vertical gate configuration counterpart [21]. A small positive gate voltage is enough to break the potential barrier and start conduction at high saturation currents in this design which makes it suitable for fast power switching applications.

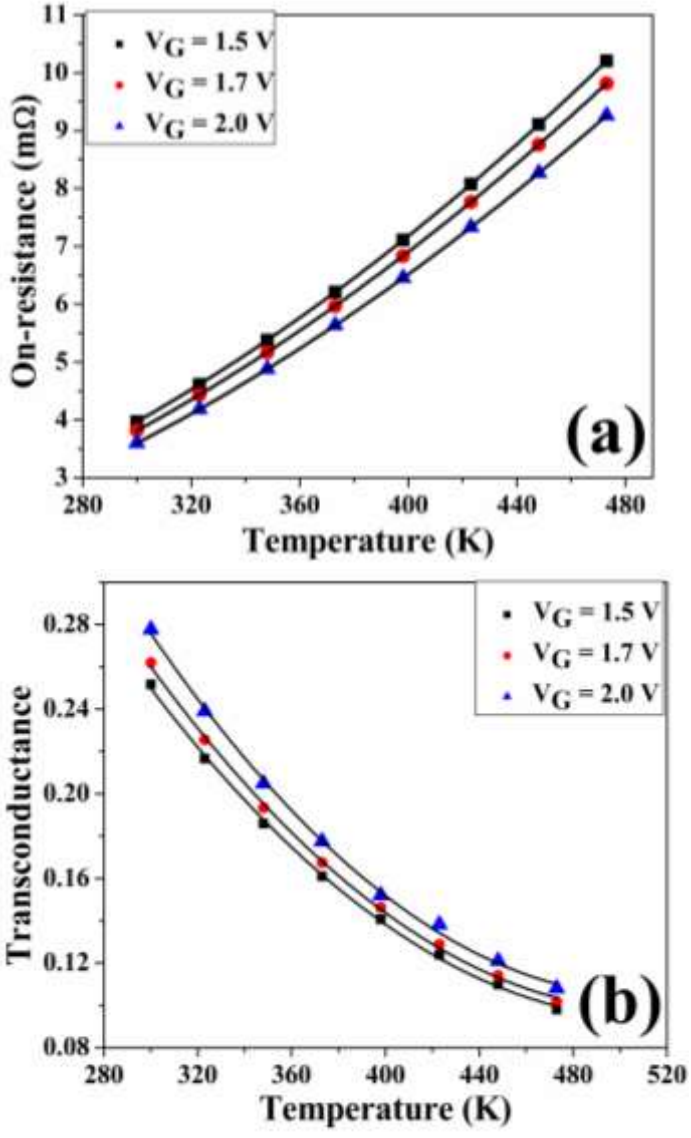

Figure 3. (a) Temperature dependent on-resistance values obtained for a VJFET with 1.45 µm channel width at diiferent gate voltages (b)Temperature dependent transconductance values obtained for a VJFET with 1.45 µm channel width at diiferent gate voltages.

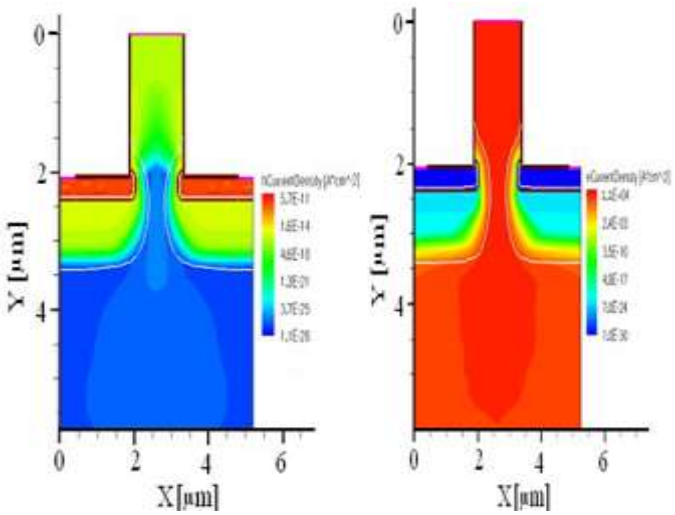

Figure 4. Temperature induced variations in electron (right) and hole (left) densities.

The saturation current values were calculated at temperatures ranging from 300 K to 473 K for channel widths including 1.25, 1.35, and 1.45.The values were calculated for gate voltages of 1.5 V, 1.7 V and 2.0 V. It was observed that the saturation current increases with decreasing the temperature while it decreases with decreasing the channel width. The maximum saturation current value of1.23 A at 300 K was observed with gate voltage value of 2.0 V when the channel width was 1.45 µm while the minimum saturation current value of 0.38 A was observed at 473 K with channel width of 1.25 µm and gate voltage of 1.5 V which is approximately 30% lower than the maximum value recorded for a similar structure. The low on-resistance is the characteristics of normally-on JFETs only, but they are not preferred in most of the applications because of high system safety requirements [23].

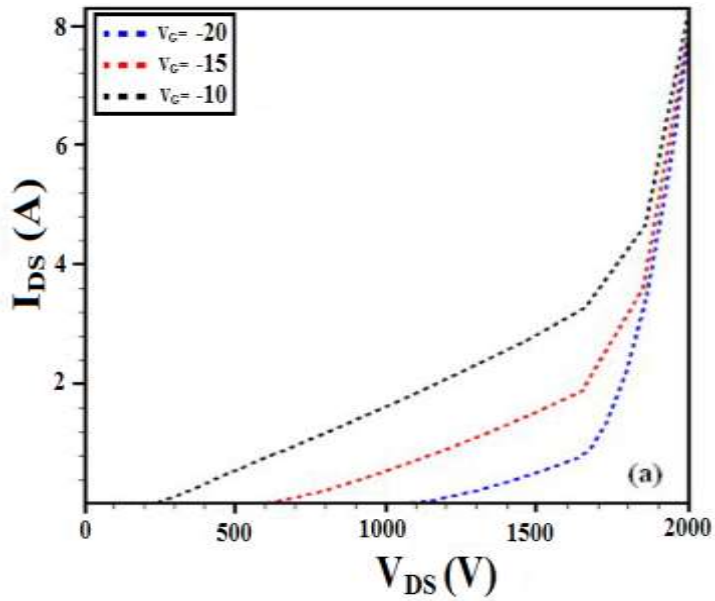

Figure 5. The blocking IDS-VDS characteristics curve of normally-off 4H-SiC VJFET for a 1.25 µm channel width at 300K.

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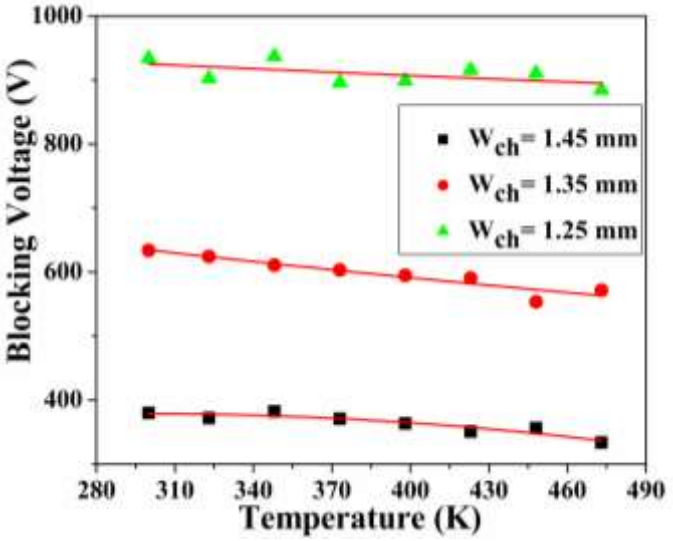

Figure 6. Temperature dependent blocking voltages for three different channel widths.

The development of inherently safe gate drivers is particularly desired in normally-on devices in order to guarantee the system safety which increases the overall cost of the system [23].But the structure discussed in this paper eliminates these requirements by offering a sufficiently low on-resistance with Normally-off characteristics which in this case is as low as 3.6 m Ω for a 1.45 μm wide channel with a gate voltage of 2V at 300 K. While the saturation current decreases at 475 K due to the temperature induced thermal scattering increasing the on-resistance of the device. Fig. 3(a) illustrates the influence of temperature on device's on-state performance. The saturation current decreases at high temperature obviously due to the reduction in carrier mobility [24].

The JFET structure, temperature and applied voltages influence the device performance in terms of its transconductance (gm). The maximum gm value of 0.27 was achieved at room temperature for maximum positive gate voltage applied to wider channel VJFET. Fig. 3 (b) gives a temperature versus gm graph for a range of gate voltages from 1.5 to 2 V.

Electron and hole density varies at different temperatures for a given VG as shown in Fig. 4. The electron current is more influenced by the temperature as compared to hole current. No significant decrease in hole current was observed at high temperature as expected.

To achieve the high blocking voltage capability, 2000 V was applied to the drain. Fig. 5 gives the blocking IDS-VDS characteristics curve of normally-off 4H-SiC VJFET for a 1.25 μm channel width at 300K.

It is clear from the figures that the blocking voltage increases with increasing the negative voltage. The high negative gate voltage establishes high potential barrier which is responsible for high blocking capability.

Elimination of vertical gates reduces device's blocking capability due to lower control over channel mobility.

However a reduced channel width (1.25 um) offers a maximum Vbl of 933 V for -20 V of VG at room temperature which is satisfactory for such a gate design. The device loses control over channel mobility at high temperature decreasing the overall blocking capability as a consequence of thermally generated carriers [25] as shown in Fig. 6. Hence, a large blocking current flows through the channel even in a device with shorter channel widths. The minimum blocking current value of 5.02 A was observed at 473 K with channel width of 1.25 μm and gate voltage of -20 V which is approximately 47.74 % lower than the maximum value recorded.

V. CONCLUSION

2D numerical simulations were performed using powerful tools presented by Sentaurus TCAD. The forward and blocking characteristics were simulated to observe the influence of temperature, channel width and gate voltages. The physics based models and parameters used for device simulation mainly depend on device geometry and doping.

It is a most comprehensive study giving a detailed insight into the JFET'S behavior for a novel structure exploiting the p+ body regions as gates eliminating the requirement of vertical gates.

In forward operation, the simulation results show that lateral gate geometry has a direct influence on the saturation current and the current increases with increasing the gate voltage because of the reduced potential barrier as a consequence of the absence of vertical gates.. The maximum saturation current of 1.23 A corresponding to a low on-resistance of 3.6 mΩ was observed at gate voltage of 2.0 V. The temperature effect was studied is detail and the simulation results show that the forward saturation current decreases with increasing the temperature because of reduction in carrier mobility. Channel width has an important effect on the saturation current and high drain currents are achieved with larger channel openings. In blocking mode, the effect of negative gate voltage, channel width and temperature on blocking characteristics was studied. The design structure shows a comparatively low blocking capability at even high negative voltage and maximum blocking voltage of 933 V was observed at VG = -20 V; the reason being its body gate configuration. The blocking voltage is very sensitive to temperature because of high thermally generated carriers which are responsible for decrease in blocking current. Also, channel width affects the blocking characteristics and the results show that shorter channel width is more capable to provide high blocking voltages.

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